**Dept. of CSE, Bennett University**

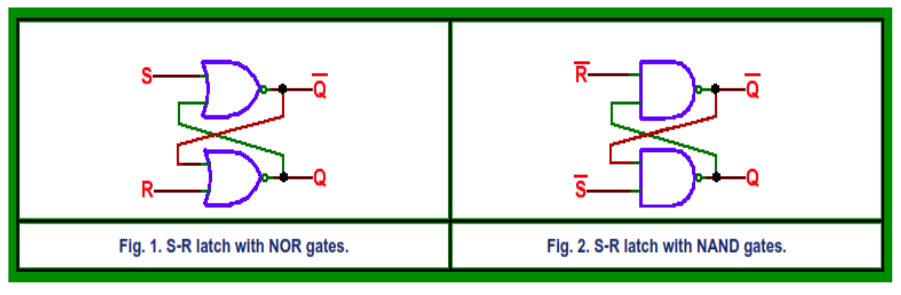
**Digital Design – ECSE 108L**

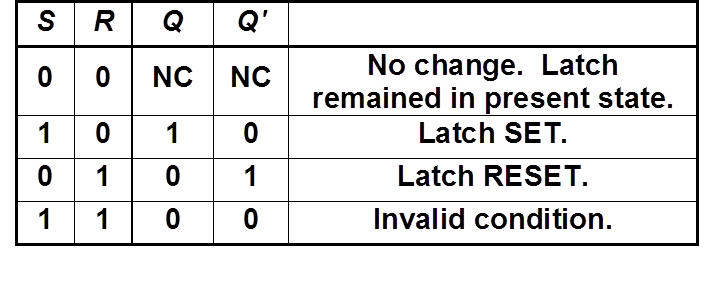
**Lab Assignment – 8**

**Sequential Circuits: S-R latch and flip flop**

In this lab we will learn about the sequential logic circuits. These circuits can act as a memory unit.

**Q 1.** An SR latch (Set/Reset) is an asynchronous device: it works independently of control signals and relies only on the state of the S and R inputs. The symbol, the circuit using NOR gates, and the truth table are shown below.





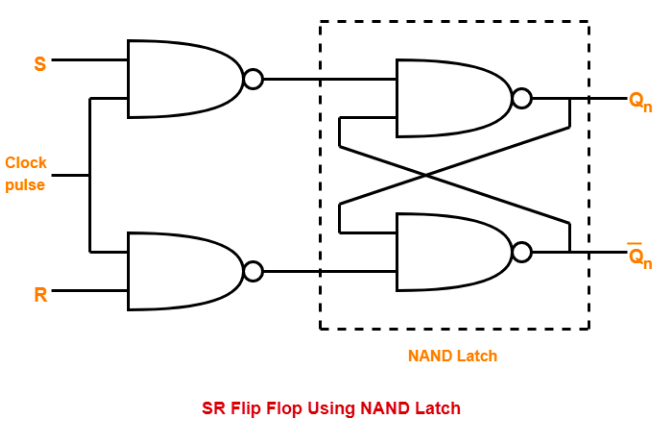
**Table 1: S-R latch truth table**

Based on the above figure and truth table, complete following tasks.

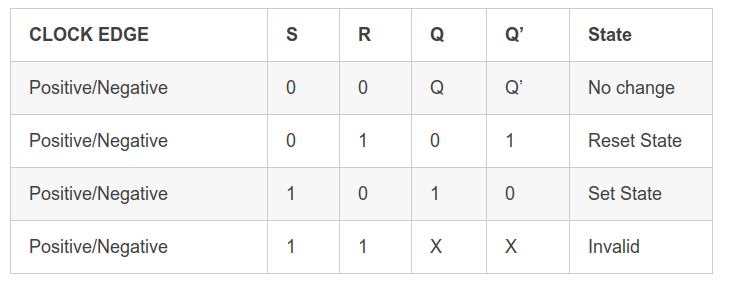
1. Generate the Boolean expression for the S-R latch from the truth table given in Table-1.
2. Write a module for NOR gate and develop a structural verilog code for the S-R latch using the NOR gate module.
3. Validate the code via a suitable Testbench code.

**Q 2**. In S-R latch we do not use a clock. Now if we add an additional clock at input so that the S and R inputs are active only when the clock is high. When the clock goes low, the state of flip-flop is latched and cannot change until the clock goes high again. This clocked addition in S-R latch is also called the S-R flip flop. Use the below given figure and truth table for S-R flip flop.

We can add a clock in put in NAND latch in Figure 2, and can convert in S-R flip flop using NAND gates as: (similar results can be achieved via NOR Latch)



**Figure 3: S-R Flip flop using NAND latch**



**Table 2: S-R flip flop truth table**

1. Generate the Boolean expression for the S-R flipflop using K-map and truth table given in Table 2.
2. Write a verilog module for NAND gate and utlize it to develop a structural verilog module for S-R flip flop as per figure 3.
3. Validate it using suitable Test bench.

**Q 3**. We can also develop a behavioral modeling based verilog code for the S-R latch. Here we can use the if-else logic to assign values for output based on the input conditions.

For example the the condition S = 1 or H, R = 0 or L then Q = 1 and Q’ = 0 cab be expressed under a begin block using if condition as:

*if(S == 1 & R == 0 )*

*begin*

*Q <= 1;*

*Q\_bar <= 0;*

*end*

Similar code can be developed for rest of the conditions.

1. Develop a behavioral verilog code using if-else slatemets for S-R latch.
2. Varify it with a suitable testbench code.

**Q 4**. develop a similar behavioral code and test bench for S-R flip flop using if-else condition as per question 3.

**Submission Instructions:**

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* Prepare the submission file according to the following process:

1. Copy the Verilog code, the Test Bench Code in a Word File.

2. Take the ScreenShot of Waveform and paste into the same word file.

3. Repeat Step 1 and 2 for all the programs

4. Copy and Paste all the Verilog code, Testbench Code and Waveform into a single

word file as 1\_verilog, 1\_TestBench, 1\_Waveform, 2\_verilog, 2\_TestBench,

2\_Waveform... etc.

1. Convert it into pdf file, name it as RollNo\_Assignment# (Example: E20CSE001\_

Assignment3.pdf).

1. Submit your file on LMS within the deadline.

* Write your Name and Roll No. as comment before starting of each program. Keep in

mind this is Mandatory. Failing which you may lose your marks.

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* Make it sure that in each program, you have mentioned enough comments regarding the

explanation of program instructions.

* Each student will submit their assignment on their corresponding group slot only.

 Late submission will lead to penalty.

* Any form of plagiarism/copying from peer or internet sources will lead penalty.
* Following of all instructions at submission time is mandatory. Missing of any instructions

at submission time will lead penalty.